REMARKS

In the Office Action of March 9, 2005, claims 1-46 were presented for examination. Claims 17 and 18 were allowed. Claims 1, 11, 19-20, 27, 34-40, and 42-45 were rejected. All other clams were merely "objected to." Herein, no claims are cancelled or added. Claims 36-40 and 42-45 are amended. Reconsideration is requested.

The applicant notes that claims 17 and 18 are allowed, and that claims 2 to 10, 12 to 16, 21 to 26, 28 to 32, 41 and 46 are objected to as being dependent on a rejected base claims, but would be allowable if rewritten in independent form. Rewriting these claims is deferred as unnecessary in light of the allowability of the independent claims as discussed below.

Claim Rejections – 35 U.S.C. §112

Claims 36-40 and 42-45 have been rejected as lacking antecedent basis for "the channel." To overcome the rejection of claims 36 to 40 and 42 to 45 under 35 U.S.C. §112, such claims have been revised to remove the reference to the term "the channel." However, since claims 40 and 45 are limited to the clear code being selected to correct for voltage offset in a channel in which the DAC is provided, the second occurrence of the term "the channel" has been revised to introduce the term "channel" with the indefinite article, being a channel in which the DAC is provided. In claim 38 the reference to "the corresponding DAC" has been corrected to "the DAC". Accordingly, this rejection now should be withdrawn.

Claims Rejections – 35 U.S.C. §102(b)

Claims 1, 11, 19, 20, 27, 34 to 40 and 42 to 45 have been rejected under 35 U.S.C. 102(b) as anticipated by Bowers. Reconsideration is requested.

The Office Action states that the invention of claims 1, 11, 19, 20, 27, 34 to 40 and 42 to 45 is anticipated by the disclosure of Bowers '123. However, this conclusion is incorrect and based on a misreading of the reference.

The Office Action states that Bowers discloses an integrated circuit comprising a digital-to-analog converter, which is interpreted as the DAC portion 48. The Office Action further asserts that Bowers discloses an alleged clear or reset code register 42 for storing an alleged predetermined digital code or reset code value, and in support of these contentions the Office

Action refers to column 6, lines 65 to 67. The Office Action also contends that Bowers discloses a control circuit, which is said to be a CMOS control circuit which is allegedly described at column 3 from line 6 onwards. The control circuit is said to be responsive to an alleged clear/reset command signal which is allegedly produced by a circuit 10 in Fig. 4 for, according to the Office Action, transferring the alleged predetermined digital clear or reset code value from an alleged clear code register 44,46 to the DAC portion 48 so that the DAC outputs an analog output signal, which is allegedly identified in Fig. 4 as "ANALOG OUT", which is to correspond to the clear code.

With these statements in mind, Principal has considered the disclosure of Bowers from first word to last, and after doing so is at a complete loss to understand how and where the Examiner thinks he has found the features of claim 1 in Bowers.

Bowers fails entirely to disclose an integrated circuit, or any type of circuit which comprises one or more clear code registers for storing a digital clear code. Furthermore, there is no disclosure in Bowers of a control circuit which is responsive to a clear code signal for transferring the clear code from the clear code register to the DAC. The circuit of Bowers has nothing to do with clear codes or their transfer in response to a clear code signal. Bowers is concerned, rather, with providing a power-on reset circuit which initiates a reset signal when the voltage of the power supply is low during power-up, and terminates the reset signal in response to the power supply voltage exceeding a reference voltage. There is no disclosure, nor is there any suggestion in Bowers that the circuit of Bowers could be responsive to a clear signal. The circuit of Bowers is solely concerned with producing a reset signal for preventing operation of the circuit until the supply voltage has exceeded a safe working level.

In Fig. 4, Bowers discloses digital circuitry 42 which includes registers 44 and 46, which are connected to an analog circuit section 48 which produces an analog output signal, which corresponds to digital values stored within the registers 44 and 46, see column 6, lines 51 to 58. The block 10 in Fig. 4 represents the power-on reset circuit which is illustrated in Fig. 2, and which provides the reset signal on an output terminal 14, until the supply voltage has exceeded a reference voltage – i.e., which is the safe working voltage. The reset signal from the power-on reset circuit 10 is used to set digital values within the registers 44 and 46 to respective predetermined values, typically zeros, see column 6, lines 64 to 67. The registers 44 and 46 have

no function other than to be reset to zeros in response to the reset signal for producing a corresponding analog output signal at the ANALOGUE OUTPUT.

There is absolutely no disclosure, and no suggestion, that the registers 44 and 46 store a clear code. Moreover, there is neither disclosure nor any suggestion in Bowers of the power-on reset circuit 10 being responsive to a clear signal. As mentioned above, the power-on reset circuit 10 of Bowers merely outputs a reset signal which sets the digital values in the registers 44 and 46 to predetermined values, typically zeros.

Manifestly, therefore, the invention of claim 1 is novel over Bowers and the rejection should be withdrawn against claim 1.

Since claims 2 to 16 and claims 35 to 41 depend either directly or indirectly on claim 1, once the Examiner is satisfied of the allowability of claim 1, claims 2 to 16 and claims 35 to 41 are likewise allowable.

Claim 19 is directed towards a method for setting a DAC of an integrated circuit to a clear condition in response to a clear signal. The method of claim 19 comprises method steps which correspond directly with the features claimed in claim 1. Accordingly, similar comments apply for claim 19 as apply for claim 1. Therefore, claim 19 is novel and allowable.

Since claims 20 to 34 and 42 to 46 depend either directly or indirectly from claim 19, once the Examiner is satisfied of the allowability of claim 19, claims 20 to 34 and claims 42 to 46 are likewise allowable.

All rejections therefore should be withdrawn.

In view of the above, the Application should now be in order for allowance, and allowance is respectfully requested.

If this communication is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to deposit account No. 23/2825.

Respectfully submitted,

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